We claim:

1. A differential switched capacitor digital-to-analogue (DAC) circuit comprising first and second differential signal circuit portions for providing respective positive and negative signal outputs with respect to a reference level, and having at least one first reference voltage input and at least one second reference voltage input for receiving respective positive and negative references with respect to said reference level; each of said first and second circuit portions comprising an amplifier with a feedback capacitor, a second capacitor, and a switch to switchably couple said second capacitor to a selected one of said reference voltage inputs to charge the second capacitor and to said feedback capacitor to share charge with the feedback capacitor, and wherein said switch of said first circuit portion is further configured to connect said second capacitor of said first circuit portion to share charge with said feedback capacitor of said second circuit portion, and wherein said switch of said second circuit portion is further configured to connect said second capacitor of said second circuit portion to share charge with said feedback capacitor of said first circuit portion.

2. A differential switched capacitor digital-to-analogue (DAC) circuit as claimed in claim 1 further comprising a switch controller to control said switches of said first and second circuit portions, said switch controller being configured to control each of said switches to perform repeated charge-dump cycles in which each said second capacitor is charged and then shares its charge with a said feedback capacitor, said switch controller being further configured to control said switch of said first circuit portion to alternate, every second of said charge-dump cycles, between connection of said second capacitor of said first circuit portion to share charge with said feedback capacitor of said first circuit portion and connection to share charge with said feedback capacitor of said second circuit portion, and to control said switch of said second circuit portion to alternate, every second of said charge-dump cycles, between connection of said second capacitor of said second circuit portion to share charge with said feedback capacitor of said second circuit portion and connection to share charge with said feedback capacitor of said first circuit portion.

3. A differential switched capacitor digital-to-analogue (DAC) as claimed in claim 2 wherein said switch controller is configured to control said switches to alternate charging of said second capacitor between said first and second reference voltage inputs.

4. A differential switched capacitor digital-to-analogue (DAC) as claimed in claim 3 wherein said switch controller is configured to alternate said second capacitor charging every second of said charge-dump cycles, in synchrony with said charge-sharing alternation.

5. A differential switched capacitor digital-to-analogue (DAC) circuit as claimed in claim 1 further comprising a switch controller to control said switches of said first and second circuit portions, said switch controller being configured to control each of said switches to perform repeated charge-dump cycles in which each said second capacitor is charged and then shares its charge with a said feedback capacitor, said switch controller being further configured to control said switch of said first circuit portion to alternate, according to a pseudo-random sequence, between connection of said second capacitor of said first circuit portion to share charge with said feedback capacitor of said first circuit portion and connection to share charge with said feedback capacitor of said second circuit portion, and to control said switch of said second circuit portion to alternate, according to a pseudo-random sequence, between connection of said second capacitor of said second circuit portion to share charge with said feedback capacitor of said second circuit portion and connection to share charge with said feedback capacitor of said first circuit portion.

6. A differential switched capacitor digital-to-analogue (DAC) as claimed in claim 2 wherein said switch controller has a digital signal input, and wherein said switch controller is configured to control said switches to charge said second capacitors responsive to a signal on said digital signal input.

7. A differential switched capacitor digital-to-analogue (DAC) as claimed in claim 1 further comprising, for each of said first and second circuit portions, a plurality of said second capacitors, each switchably connectable to a selected one of said reference

voltage inputs, to said feedback capacitor of said first circuit portion, and to said feedback capacitor of said second circuit portion.

8. A differential switched capacitor digital-to-analogue (DAC) as claimed in claim 1 further comprising an amplifier switch for each of said first and second circuit portions configured to effectively exchange the amplifiers of said first and second circuit portions.

9. A differential switched capacitor circuit comprising positive and negative circuit portions to provide respective positive and negative differential signal outputs based upon positive and negative references, each of said positive and negative circuit portions comprising an operational amplifier with a feedback capacitor and at least one switched capacitor connectable to one of said positive and negative references to store charge and to one of a positive and negative signal node to substantially dump said stored charge to a said feedback capacitor, and wherein said switched capacitors of said positive and negative circuit portions are switched according to an eight phase clocking scheme comprising four successive charge-dump cycles in which said switched capacitors are connected to a said positive signal node for a first pair of said charge-dump cycles and to a said negative signal node for a second pair of said charge-dump cycles.

10. A method of operating a differential digital-to-analogue (DAC) circuit to reduce signal dependent loading of a reference source associated with the DAC circuit, the DAC circuit comprising positive and negative signal processing devices each with a feedback capacitor coupled to a respective positive and negative signal node and a each having a second capacitor switchably couplable to said reference source for charging and to a said signal node for dumping charge to a said feedback capacitor, the method comprising repeatedly:

coupling said second capacitors to said reference source for charging; and

coupling said second capacitors to alternate ones of said positive and negative signal nodes for dumping stored charge to a said feedback capacitor;

such that on average over a plurality of charge-dump cycles charge loading of said reference source by said DAC circuit is substantially constant.

11. A method of operating a differential DAC circuit as claimed in claim 10 wherein each of said second capacitors is coupled to an alternate one of said positive and negative signal nodes every second charge-dump cycle.